REMARKS

The application contains claims 4-7, 9-12, 17-20, 23, and 25-26. Claims 4-7 and 9 are allowed. In view of the foregoing amendments and following remarks, Applicant respectfully requests allowance of the application.

CLAIM OBJECTIONS

The foregoing amendments are provided to overcome the claim objections made in the Office Action. Accordingly, Applicant respectfully requests withdrawal of the claim objections.

PRIOR ART REJECTIONS

Claims 10-12, 17-20, 23, and 25-26 stand rejected based on prior art. Applicant respectfully requests withdrawal of these outstanding rejections because the prior art does not disclose, teach, or suggest all elements of the pending claims.

Claims 10-12 are allowable over the cited art.

Claims 10 and 12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshioka et al. (U.S. Patent No. 4,394,729). Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshioka in view of IBM Technical Disclosure Bulletin NN9204269 ("IBM"). These rejections are respectfully traversed.

Amended claim 10 recites, in part:

> determining, with reference to other instructions read previously from the instruction pipestage, whether a return address is available to the instruction pipe prior to expiration of the round-trip communication latency period with the return-stack buffer;
>
> if the return address is available immediately upon receipt of the return instruction at the instruction pipestage, forwarding the return address to a next pipestage during a next clock cycle, and
>
> if not, stalling processing of the return instruction until the round-trip communication latency period expires and forwarding a received return address thereafter.

Yoshioka does not disclose, teach, or suggest this subject matter. The Office Action alleges that Yoshioka's determination of "whether a previous subroutine jump/call instruction has set BANKV(CNT) = 1 and CNT <= 8" is equivalent to the determination of "whether a return address is available to the instruction pipe prior to expiration of the round-trip communication latency period with the return stack buffer" as recited in claim 10. Applicant respectfully disagrees. Yoshioka discloses a compiler that uses a register to store the return address for return after branch, rather than from the stack area developed on a memory, to increase the processing speed. Yoshioka discloses that BANKV(CNT) is set to 1 when CNT <= 8 and RAHV =1, which means that "there is an empty register which can be used by the register allocation function by the previous NOP instruction." Yoshioka, col. 8, lines 54-66. BANKV(CNT) = 1 means that the nest level of the subroutine is consistent. Id. at col. 9, lines 10-12. CNT <= 8 means that "the nest level of a subroutine does not reach the upper limit and empty banks present." Id. at col. 8, lines 60-63. Thus, the condition "BANKV(CNT) = 1 and CNT <= 8" has nothing to do with the round-trip communication latency period. In fact, Yoshioka says nothing about the timing problem that arises due to round-trip communication latencies between the instruction pipe and the RSB and/or maintaining timing synchronism between the instruction pipe and the RSB.

Moreover, in col. 9, lines 6-30, Yoshioka discloses simply that the return address is read from the register if the condition "BANKV(CNT) = 1 and CNT <= 8" is met. If this condition is not met, it is assumed that the return address was stored in the stack buffer, and the program reads it from the stack area. Id. at col. 9, lines 18-21. Yoshioka, however, says nothing about "forwarding the return address to a next pipestage" and "stalling processing of the return instruction." Thus, Yoshioka fails to disclose, teach, or suggest the subject matter of claim 10.

IBM does not make up the deficiencies of Yoshioka. As the Office Action stated, IBM discloses "determining whether the return instruction requires access to return stack buffer in excess of an access allocation for the instruction pipe" and "if two return instructions are close to each other, then the second return will be have to be stalled since only one should access the stack at a time." IBM, however, discloses nothing about the round-trip communication latency period. Moreover, in IBM, whether to stall processing of the return instruction is not conditional upon "if the return address is available immediately upon receipt of the return

instruction at the instruction pipestage" as recited in claim 10. Accordingly, independent claim 10 is allowable over the cited art. Claims 11-12, which depend from independent claim 10, are also allowable over the cited art. These § 102(b) and § 103(a) rejections should be withdrawn.

Claims 17-20 are allowable over the cited art.

Claim 17 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Pickett (U.S. Patent No. 5,968,169). Claims 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pickett in view of Sproch et al. (U.S. Patent No. 6,247,134). These rejections are respectfully traversed.

Amended claim 17 recites, in part:

> a first instruction pipe, comprising a first plurality of cascaded pipestages, the first instruction pipe including a return stack buffer, and
>
> a second instruction pipe, comprising a second plurality of cascaded pipestages, the second instruction pipe being in communication with the return stack buffer of the first instruction pipe through a communication path having a communication latency that is different from the communication latency between the first instruction pipe and the return stack buffer.

Pickett does not disclose, teach, or suggest this subject matter. In particular, Pickett does not disclose a return stack buffer being included in the first instruction pipe and also in communication with a second instruction pipe. Rather, Pickett's return stack is included in the branch prediction unit 220. Neither the multiple decode units nor the multiple functional units, which are alleged to be equivalents of the first and second instruction pipes by the Office Action, include the branch prediction unit. Sproch does not overcome this deficiency of Pickett. Sproch's system only includes one pipeline. Thus, independent claim 17 is patentable over the cited art. Accordingly, claims 18-20, which depend from independent claim 17, are also patentable over the art.

Claim 23 is allowable over the cited art.

Claim 23 stands rejected under 35 U.S.C. § 102(b) as being anticipated by IBM. This rejection is respectfully traversed.

Claim 23 recites, in part:

> determining whether the pipestage processed a prior return instruction faster than a latency period for round trip communication between the pipestage and the return stack buffer,
>
> if so, stalling the downstream pipestages until the period for processing a prior return instruction equals the round trip communication latency period.

As set forth in Applicant's April 26, 2004 Preliminary Amendment, IBM does not disclose, teach, or suggest this subject matter of claim 23. IBM states that "if a return is followed by another return instruction before the first one completes, you need to hold the second return in decode until the first one completes in write back stage." This "before the first one completes" refers to execution time of a return instruction (or the time it takes to execute a return instruction), but not the round-trip communication latency period with the return stack buffer. Thus, IBM fails to disclose, teach, or suggest stalling the pipestages until the period for processing a prior return instruction equals the round trip communication latency period. Accordingly, IBM can not anticipate claim 23., and claim 23 is patentable over the cited art.

Claims 25-26 are allowable over the cited art.

Claim 25 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Armstrong (U.S. Patent No. 4,394,729). Claim 26 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Armstrong in view of Sproch. These rejections are respectfully traversed.

Amended claim 25 recites, in part:

> a plurality of pipestages connected in cascade,
>
> first and second registers provided between first and second pipestages of the plurality,
>
> the first register to store a return address received from the first pipestage during receipt of a call instruction,
>
> the second register to store a return address received from a return stack buffer, and
>
> a selector coupling the first and second registers to the second pipestage.

Armstrong does not disclose, teach, or suggest this subject matter. The Office Action contends that FIG. 4A illustrates first and second registers provided between first and second pipestages of the plurality of pipestages connected in cascade; one register being the counter register and

another being the register at the top of the register file stack. Applicant respectfully disagrees. FIGs. 4A-D illustrate the contents of the jump return stack (JRS) 30, and FIG. 2 illustrates the structure of the JRS. See Armstrong, Brief Description of the Drawings. As illustrated in FIG. 1, the JRS is not provided between the first and second pipesages of the plurality. Thus, Armstrong fails to disclose "first and second registers provided between first and second pipestages of the plurality" as recited in claim 25.

Additionally, Armstrong does not disclose, teach, or suggest "the first register to store a return address received from the first pipestage during receipt of a call instruction and the second register to store a return address received from a return stack buffer." Rather, Armstrong merely discloses that the counter/register always stores the latest entry into the top of the memory stack so that it is immediately available to the control register. Thus, Armstrong fails to disclose, teach, or suggest the subject matter of claim 25.

Sproch does not make up the deficiencies of Armstrong for at least the reason that it fails to disclose, teach, or suggest "the first register to store a return address received from the first pipestage during receipt of a call instruction and the second register to store a return address received from a return stack buffer." In fact, Sproch says nothing about the return stack buffer.

Accordingly, independent claim 25 is allowable over the cited art. Claim 26, which depends from independent claim 25, is also allowable over the cited art. These § 102(b) and § 103(a) rejections should be withdrawn.

CONCLUSION

In view of the above amendments and remarks, Applicant respectfully submits that the present application is now in condition for allowance. A timely Notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any aspect of the application.

The Office is authorized to charge any fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,

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